Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT –**
4. **V-**
5. **OUTPUT**
6. **V+**

**.029”**

**.029”**

**1 6**

**5**

**4**

**3**

**2**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .029” X .029” DATE: 1/8/19**

**MFG: NATIONAL THICKNESS .028” P/N: LM710**

**DG 10.1.2**

#### Rev B, 7/1